Technical Note

Intrinsic Jitter Correction for Jitter Measurements

MP2100A

BERTWave Series

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1. Introduction

To cope with the rapid increases in data volumes, data centers are introducing high-speed interconnects with transmission speeds faster than 10 Gbit/s between servers. However, in conflict with these speed increases, there is increasing demand for lower power consumption as well as cost reductions. Furthermore, higher jitter levels and degraded waveforms are becoming a problem. Various measuring instruments, such as Sampling Scopes (Eye Pattern Analyzer) and BERTs are being used to classify and analyze jitter components such as DJ, RJ, etc., affecting communications quality over fibre channel, 10GbE, USB, PCI, etc. Increasing bit rate speeds require higher accuracy from measuring instruments used for these measurements, but the dependency of sampling oscilloscopes on the instrument's own intrinsic jitter in the trigger clock circuits and its effect on the measurement results cannot be ignored sometimes.

This document explains how to correct intrinsic jitter and perform more accurate measurements using the MX210001A Jitter Analysis Software.

2. Classification of Jitter Components using Sampling Scope

Jitter analysis is becoming an increasingly important topic for engineers looking to increase the transmission speed of digital electronic circuits. As the data transmission speed is increased, the size of the Eye opening decreases proportionately and the required jitter characteristics become increasingly severe. For example, the size of the Eye opening is about 1000 ps at 1GbE but is less than 100 ps at 10GbE.

The jitter is actually composed of various components. The total jitter (TJ) is composed of finite deterministic jitter (DJ) and non-finite random jitter (RJ) distributed normally. The DJ itself is composed of DDJ, which is correlated with the signal pattern, and BUJ that is not correlated with it. Moreover, the DDJ is composed of DCD related to the input/output circuit characteristics, and ISI related to the transmission path characteristics. The RJ depends on external factors such as thermal noise and has the property of being infinitely distributed in a form approaching the Gaussian distribution. Since the peak-to-peak value is distributed infinitely with time, it is expressed as rms, or the jitter standard deviation.

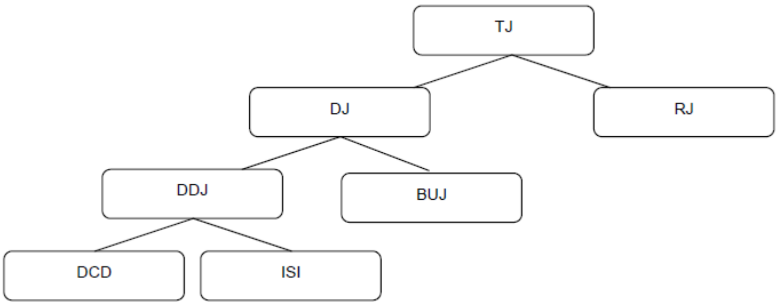

Figure 1. Classification of Jitter Types

The trigger clock circuit of the sampling oscilloscope itself also has intrinsic jitter, which is broadly the same as RJ. Although the value of this jitter in the MP2100A is kept extremely low (Technical Note MP2100A-E-E-1 “Enabling Precision EYE Pattern Analysis”), sometimes the effect of this intrinsic jitter on the measurement results cannot be ignored. The measured RJ results including the jitter RJ_D generated by the DUT and the jitter generated internally by the measuring instrument itself RJ_I can be expressed by Eq. 1.

$$RJ = \sqrt{{RJ_D}^2 + {RJ_I}^2} \qquad \text{Eq. 1}$$

Converting Eq. 1 as shown below to Eq. 2, the true value of RJ_D can be determined by subtracting RJ_I from the measured RJ.

$$RJ_D = \sqrt{RJ^2 - {RJ_I}^2} \qquad \text{Eq. 2}$$

The MX210001A Jitter Analysis Software for the MP210xA BERTWave series obtains the correction function using Eq. 2. It determines the intrinsic jitter RJ_I of the measuring instrument beforehand and automatically subtracts it from the measured jitter result to obtain the true value of RJ_D for the DUT.

3. Finding Correction Factor

The Sampling Scope intrinsic jitter is mainly due to the random jitter component RJ_I of the scope trigger clock circuit. This section explains the measurement of the RJ_I of the trigger clock circuit for use as the correction factor using an external synthesizer. Figure 2 shows the setup at intrinsic jitter measurement, assuming use of a bit rate of 10.3125 Gbit/s.

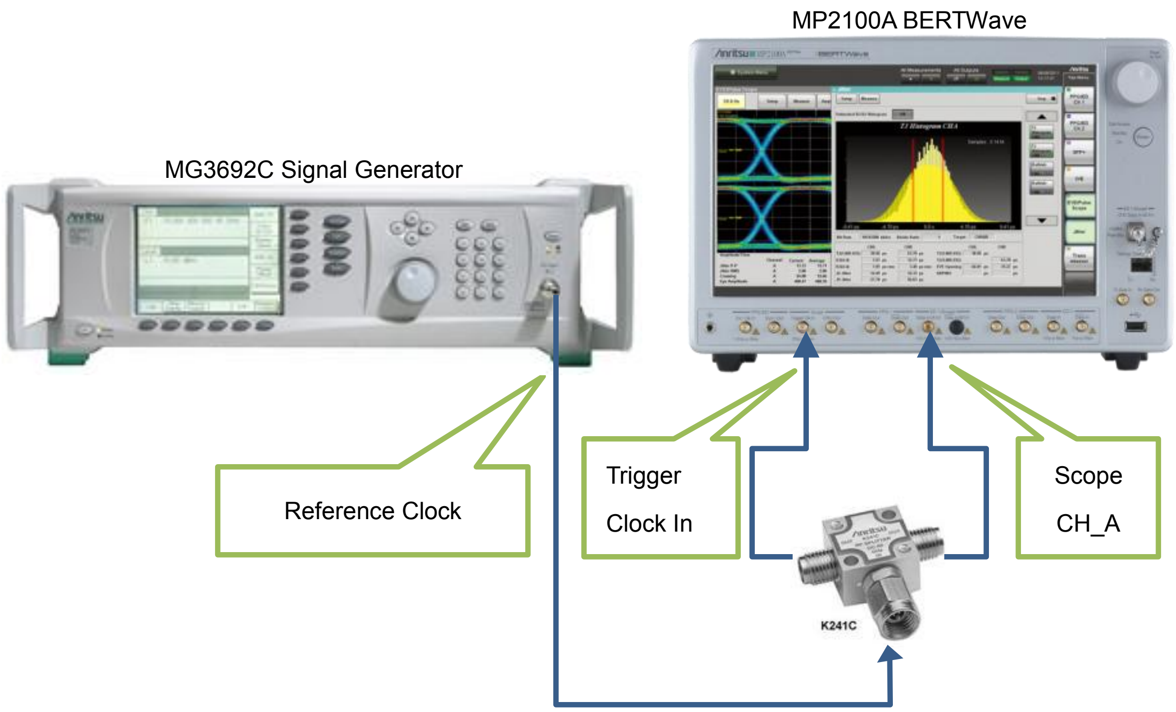

Figure 2. Intrinsic Jitter Measurement Setup for MP2100A Sampling Scope

[Procedure]

The MP2100A settings are based on the initialization defaults. To initialize, open the System Menu windows and click [Initialize].

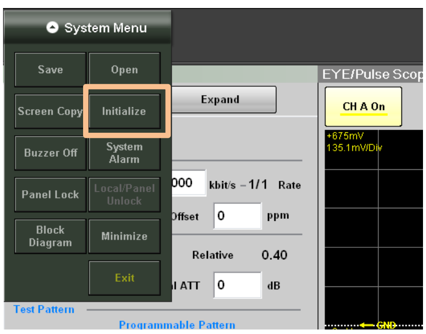

Figure 3. Initializing MP2100A

(1) Use a power splitter to divide the Signal Generator clock output and input the clocks to Trigger Clock Input and Scope CH_A connectors of the MP2100A (Fig. 2).

(2) Set the Signal Generator frequency to 5.15625 GHz (half frequency of 10.3125 GHz), the Power to +4 dBm and the Output to ON.

(3) Open the [Time] screen of the EYE/Pulse Scope and set Divide Ratio at the Rate tab to x2.

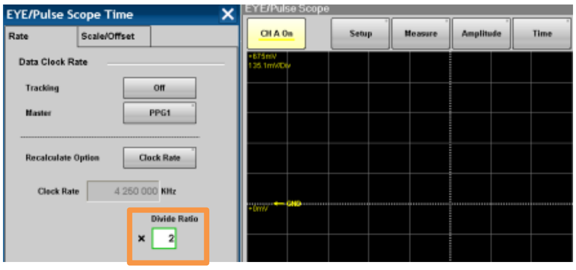

Figure 4. MP2100A Pattern

(4) Set [CH_A] of the EYE/Pulse Scope screen to ON and [CH_B] to OFF. Execute Auto Scale and confirm that the Eye pattern is displayed at the center of the screen.

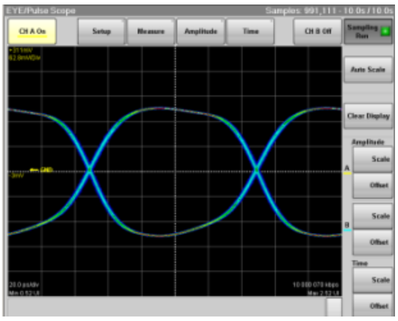

Figure 5. Clock Signal Display

(5) Open the [Jitter] screen and press the [Start/Stop] button to display the measured jitter. To assure a stable measurement result, capturing results for at least 1 Msa is recommended.

(6) The value displayed at RJ (d-d) [ps rms] the intrinsic jitter “RJ_I” of the MP2100A. Record this value and use as the correction factor as explained in section 4 below.

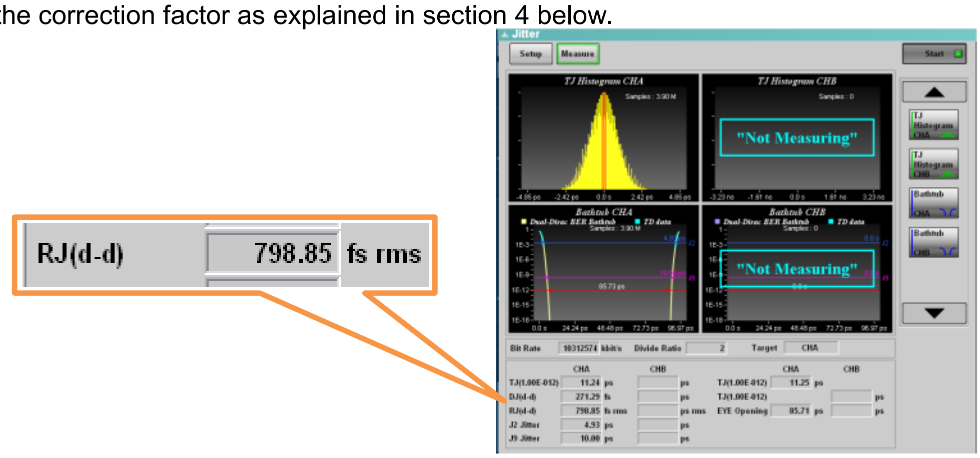

Figure 6. Measuring MP2100A RJ_I

4. Measuring DUT Jitter using MP2100A

This section explains an actual jitter measurement using a single-end 10.3125G device as an example. Figure 7 shows the MP2100A setup.

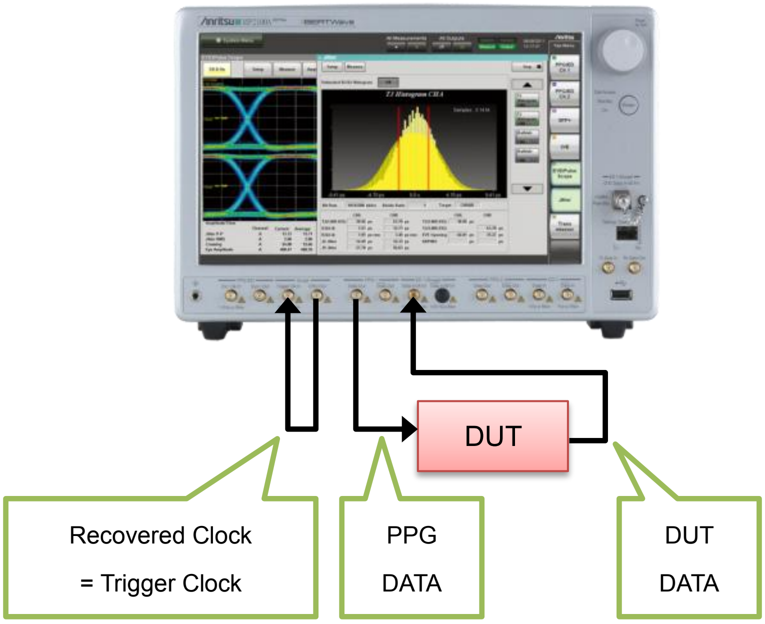

Figure 7. Electric Device Jitter Measurement Diagram using MP2100A

[Procedure]

(1) Supply a 10.3125Gbit/s, single-end, data signal from the PPG to the DUT and input the data signal output from the DUT to the CH_A Input connector of the MP2100A. This example uses a PPG PRBS 7 Test Pattern and a Data Output Amplitude setting of 0.25 V but use appropriate settings for the DUT.

(2) Connect the CRU Out and Trigger Clock In connectors of the MP2100A. This example uses Recovered Clock for Trigger Clock to operate the sampling scope, but PPG Sync. Clock Output can be used too.

(3) Open the [Setup] of the EYE/Pulse Scope screen to set Clock Recovery at the General tab to [>8.5 G].

(4) Open the [Time] of the EYE/Pulse Scope screen and set [Divide Ratio] at the Rate tab to 1.

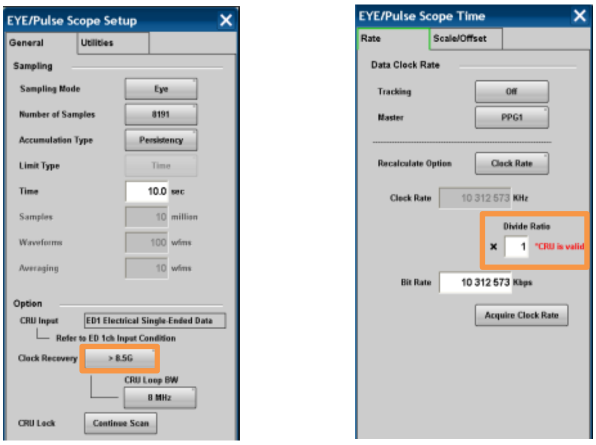

Figure 8. Setting Clock Recovery and Divide Ratio

(5) Set [CH_A] of the EYE/Pulse Scope screen to ON and [CH_B] to OFF. Execute Auto Scale and confirm that the Eye pattern is displayed at the center of the screen.

(6) Open the Jitter screen and press the [Start/Stop] button to display the measured jitter in the histogram mode.

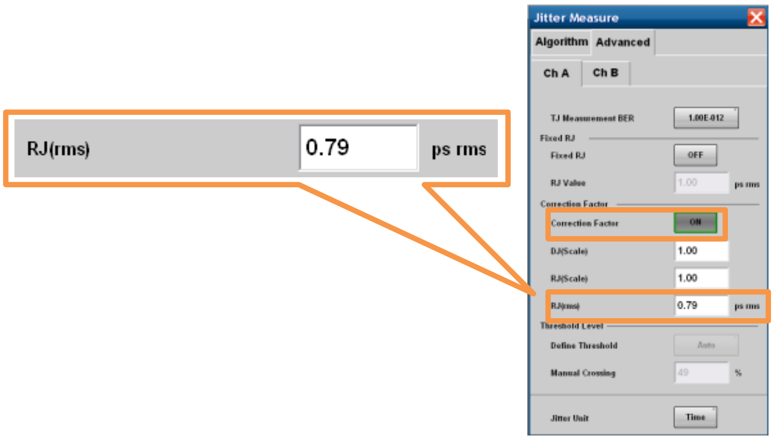

Figure 9. Setting Correction Factor

(7) Open the Jitter Measure screen and open the Ch A table of the Advanced tab. Set Correction Factor to [ON] and set the correction factor at RJ (rms) to reflect the correction factor in the measurement results. This example uses the correction factor of 0.79 ps rms measured in section 3, which reduces the measured RJ from 1.63 ps rms to 1.42 ps rms.

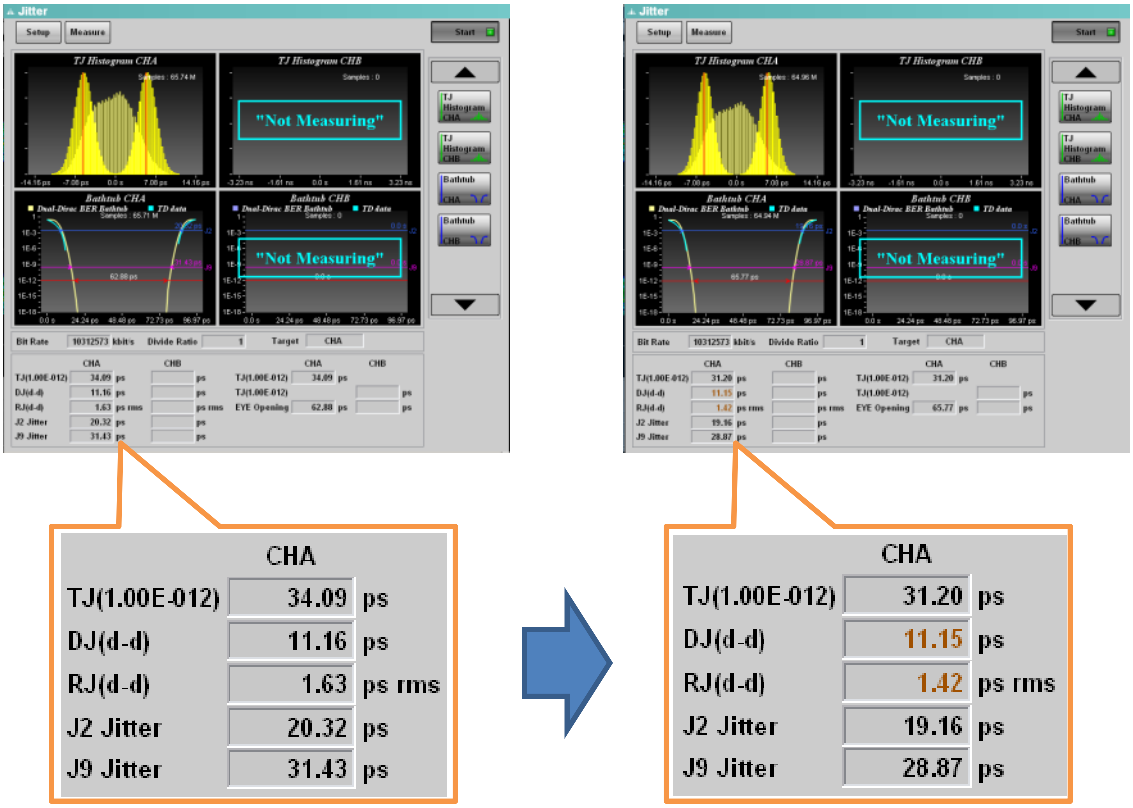

Figure 10. Measured Jitter Before and After Applying Correction Factor

5. Signal Generator Phase Noise Effect

The intrinsic jitter measurement described in Section 3 uses the MG3692A Signal Generator as the Reference Clock Source. However, since there is also jitter in this reference clock, its impact needs to be estimated. Figure 11 shows the reference phase noise of the MG3692A (with Opt-03 and Opt-04). At an offset of 1 MHz, the phase noise is –138 dBc/Hz. Based on this phase noise level, the calculated reference clock jitter is 0.04 ps rms (modulation frequency band: 1 MHz to 1 GHz), which is sufficiently small to ignore.

Figure 11. MG3690C Signal Generator Phase Noise

The reason why the modulation frequency integrated band is 1 MHz or more is because with this measurement method jitter at modulation frequencies below 1 MHz can be ignored. In the measurement setup shown in Figure 2, the measured intrinsic jitter is 0.79 ps rms. With the same setup, the jitter from the signal generator is 20 ps p-p (7.071 ps rms) and when this modulation frequency is changed from 10 Hz to 5MHz, the jitter observed at the MP2100A is shown in Fig. 12. Based on this result, at jitter modulation frequencies below 1 MHz, the observable jitter is the same whether jitter is impressed or not.

In this measurement, since the trigger clock and DUT signal are exactly the same signal, we can see that the signal source jitter is canceled up to a fixed frequency and only the measuring instrument's internal intrinsic jitter is observed.

Figure 12. MG3690C Signal Generator Phase Noise

6. Summary

This document explains how to correct measured intrinsic jitter when classifying jitter using the MP2100A sampling oscilloscope. Using this method, we can measure DUT jitter accurately without needing an expensive low phase-noise modules or circuits for Sampling Scope.

The MP2100A is an all-in-one tester supporting sampling scope and BERT functions with an optical interface. Moreover, using the MX210001A Jitter Analysis Software supports Eye Pattern, Eye Mask, BER and jitter classification analysis, improving measurement efficiency and cutting equipment costs.

[Reference]

- Anritsu Corporation, “Enabling Precision EYE Pattern Analysis”, Technical note No.MP2100A-E-E-1
- Anritsu Corporation, “Understanding Eye Pattern Measurements Application Note” , Application Note No. 11410-00533
- Anritsu Corporation, “Signal Integrity Analysis of 28 Gbit/s High-Speed Digital Signal”, Application note No. MP1800A-Signal_Integrity-E-F-1
- Wolfgang Maichen, “Digital Timing Measurements From Scopes And Probes To Timing And Jitter”, Springer, ISBN-10 0-387-31418-0

Note

Specifications are subject to change without notice.

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